Micropneumatic Digital Logic Structures for Integrated Microdevice Computation and Control

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***Abstract*—It is shown that microfabricated polydimethylsiloxane membrane valve structures can be configured to function as transistors in pneumatic digital logic circuits. Using the analogy with metal–oxide–semiconductor field-effect transistor circuits, networks of pneumatically actuated microvalves are designed to produce pneumatic digital logic gates (AND, OR, NOT, NAND, and XOR). These logic gates are combined to form 4- and 8-bit ripple-carry adders as a demonstration of their universal pneumatic computing capabilities. Signal propagation through these pneumatic circuits is characterized, and an amplifier circuit is demonstrated for improved signal transduction. Propagation of pneumatic carry information through the 8-bit adder is complete within 1.1 s, demonstrating the feasibility of integrated temporal control of pneumatic actuation systems. Integrated pneumatic logical systems reduce the number of off-chip controllers required for lab-on-a-chip and microelectromechanical system devices, allowing greater complexity and portability. This technology also enables the development of digital pneumatic computing and logic systems that are immune to electromagnetic interference. [2006-0290]**

***Index Terms*—Lab-on-a-chip, microfluidics, microprocessors, microvalves, pneumatic logic.**

I. Introduction

MICROVALVES are playing a critical role in the development of fully integrated microfluidic systems for lab-on-a-chip devices [1], [2]. Active mechanical microvalves using thermal, magnetic, piezoelectric, and pneumatic actuation mechanisms have been demonstrated [3]. The dense fabrication and parallel control capabilities of pneumatically actuated microvalves have enabled the development of devices in which hundreds of microfluidic operations can be performed in parallel [4], [5]. The normally closed monolithic polydimethylsiloxane (PDMS) membrane valves developed by our group [5] have enabled complex microfluidic control operations in lab-on-a-chip applications ranging from single nucleotide polymorphism-based DNA computing [6] to nanoliter-scale Sanger DNA sequencing [7]. The structure and function of these normally closed membrane valves are illustrated in Fig. 1(a). An etched displacement chamber in one glass wafer and a discontinuous channel structure in a second glass wafer are bonded together using a featureless PDMS membrane. Application of a vacuum to the displacement chamber through a microvalve control channel pulls the PDMS membrane away from the discontinuity, allowing fluid to flow across the discontinuity in the fluid channel [Fig. 1(b)]. The utility of these structures also extends far beyond basic valving applications in lab-on-a-chip devices.

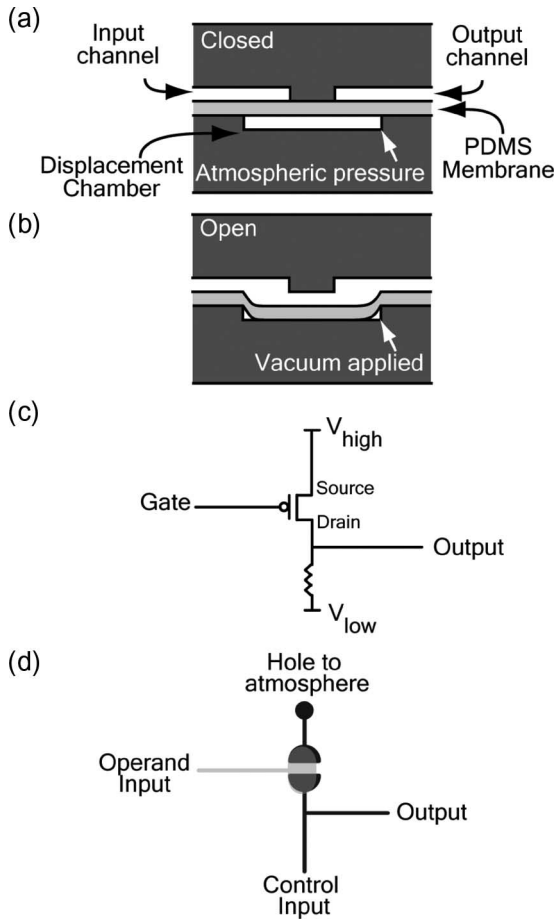

Fig. 1. (a) Cross-sectional view through a monolithic membrane valve. The valves are normally closed with the PDMS membrane resting on the valve seat. (b) The PDMS membrane is pulled into the displacement chamber, opening the valve by the application of a vacuum through the control channel. Relationship between a (c) p-MOSFET inverter and a (d) pneumatic inverter showing that PDMS membrane valves can function as pneumatic transistors. Here, and in subsequent figures, light and dark gray represent etched channel features on the two different glass layers.

Many emerging lab-on-a-chip devices require large numbers of independent on-chip valves to control complex fluidic

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operations. The large number of off-chip controllers required for such applications imposes a practical limit on the number of independent pneumatic microvalves in a microfluidic device. Several strategies for reducing the number of off-chip controllers have been presented, including valve-based fluidic demultiplexers used for addressable routing of fluid to arrays of on-chip chambers [8], [9]. Recently, we demonstrated that addressable arrays of independent microvalves can be controlled using an on-chip pneumatic demultiplexer together with bistable valve-based latching circuits [10]. In this system, microvalves are used like transistors to control airflow within microchannels and, in turn, the actuation of "working" output valves for fluid routing operations. Since these valve-based logical structures employ basic digital logic operations used in electronics, it should be possible to form networks of valves that are capable of performing even more complex logic operations to enhance device capability.

Macroscopic pneumatic logic devices were first developed in the 1960s [11], [12] and are still widely used in the automation of manufacturing processes [13], [14]. Pneumatic logical control systems are particularly useful in environments in which electronic devices present a hazard or malfunction due to hostile interferences. Recently, analogies have been suggested between pneumatically actuated microvalves and p-channel MOSFETs (p-MOSFETs) [15]. Basic logic gates such as pressure-amplifying inverters, AND gates, and OR gates have also been proposed and characterized using a variety of pneumatically actuated valves [10], [16], [17]. However, no system has been demonstrated for the large-scale integration of universal pneumatic logical structures in microfabricated devices. Analog computations such as solving the shortest path problem in mazes have been successfully performed using networks of microfluidic channels [18].

In this paper, we design and fabricate networks of pneumatically actuated microvalves that function as logic gates and demonstrate integrated combinations of these gates that perform complex digital logic operations. Fig. 1(c) and (d) illustrates the relationship between a single-transistor p-MOSFET inverter and its implementation with a normally closed pneumatically actuated microvalve circuit. With the source potential defined as 0 V, application of a negative voltage to the gate of the p-MOSFET induces a current from the positive voltage power supply ($V_{\rm high}$) to the negative supply ($V_{\rm low}$), resulting in a significant increase in the output voltage. In the equivalent pneumatic circuit, high pressure and low pressure correspond to $V_{\rm high}$ and $V_{\rm low}$, respectively. Application of a negative pressure of sufficient magnitude to the operand input of a pneumatic inverter opens the valve, resulting in a current of air from the drilled hole at atmospheric pressure (defined as 0 kPa or $P_{\rm high}$) to the gate control input which is supplied with a vacuum ($P_{\rm low}$). This increases the pressure in the output channel to a level that is insufficient for the actuation of downstream valves. In both systems, a static current (electrical or pneumatic) continuously flows when the output is high. More complex micropneumatic inverters that block this static current have been previously demonstrated [16], [17]. However, it is unclear if this feature would result in improved integration and speed, as was the case with the development of complementary metal–oxide–semiconductor technology for digital electronics.

As a test of the capabilities of these pneumatic logical structures, we have developed a variety of standard digital logic gates and combined them to function as an 8-bit ripple-carry adder. The 8-bit adder is shown to add arbitrary 8-bit binary numbers in a fully integrated glass–PDMS hybrid structure. Furthermore, we characterize the mechanical principles that allow extension of the technology to even more complex logical operations, including the integrated control of microfluidic chemical and biological analysis devices.

II. Methods

A. Device Fabrication

Device features were etched into glass wafers using conventional photolithography and wet chemical etching [19]. Briefly, 1.1-mm-thick 100-mm-diameter borosilicate glass wafers were coated with 200 nm of polysilicon using low-pressure chemical vapor deposition. The wafers were then spincoated with positive photoresist, soft baked, and patterned with the device design using a contact aligner and a chrome mask. After development and removal of irradiated photoresist, the exposed polysilicon regions were removed by etching in SF_6 plasma and the exposed regions of glass were isotropically etched in 49% hydrofluoric acid to a depth of 50 μm. After stripping the remaining photoresist and polysilicon layers, the wafers were diamond-drilled to produce 500-μm-diameter holes for pneumatic input connections. The wafers were then bonded together using a 254-μm-thick PDMS elastomer membrane (HT-6240, Rogers Corporation, Binghamton, NY).

B. Experimental Setup

Pneumatic inputs were supplied by the actuation of computer-controlled solenoid valves for the evaluation of individual microvalves, logic gates, and the adder circuits. Separate pumps were used to supply logic high (-87 kPa) and logic low (6 kPa) pressures to the solenoid valves. Pneumatic signals were conducted from the solenoid valves to the drilled chip inputs using polyurethane tubing with a 1.6-mm internal diameter and lengths ranging from 15 to 30 cm. Pressure measurements reported for single valves, logic gates, and the full adder are relative to atmospheric and were measured using a strain gauge pressure transducer (PM 100D, World Precision Instruments). Digital videos of the operation of the 4- and 8-bit adders were recorded using a charge-coupled device (CCD) camera.

C. Pneumatic Logic Gates

Pneumatic logic gates are composed of networks of valves to which pneumatic signals are applied via gate input channels. Pressures greater than -20 kPa that are applied to microvalve control channels are consistently incapable of valve actuation [5] and, therefore, represent a logic low, or the "false" value of digital logic. This is due to the adhesion force between the PDMS and the valve seat. The threshold pressure for microvalve actuation depends on the magnitude of negative

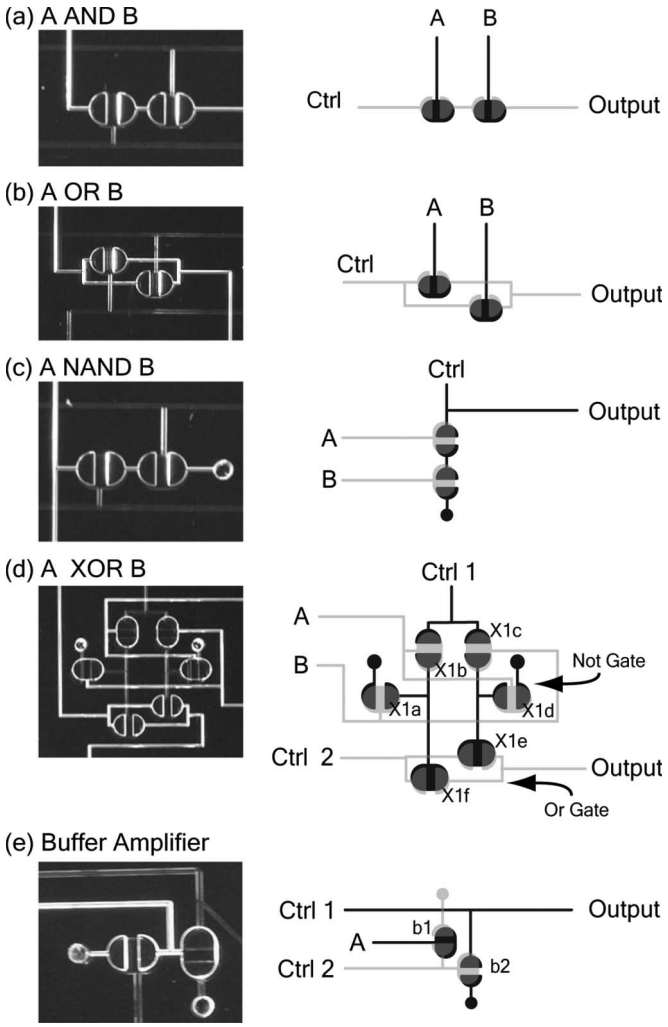


Fig. 2. Photographs and schematics of pneumatic logic gates that function similarly to MOSFET (a) AND, (b) OR, (c) NAND, (d) XOR gates, and (e) a vacuum-amplifying buffer gate. (solid circles) Drilled holes to the atmosphere serve as a source of air at atmospheric pressure (P_{high}) and vacuum applied to control channels (labelled "Ctrl") serves as a drain (P_{low}).

pressure applied to the input channel, with an upper bound of -32 kPa. Fig. 2 shows the layout of several pneumatic logic gates that operate like MOSFET logic gates. Each logic gate requires one or more gate control input channels to which constant vacuum is applied during digital logic operations. Operand gate input channels (A, B) are supplied with -87 kPa as a logic high and 6 kPa as a logic low. A pneumatic AND gate [Fig. 2(a)] is composed of two microvalves connected in series. Vacuum will only be transmitted from the control input to the output if both valves are simultaneously actuated by vacuum applied to the operand inputs. Similarly, a pneumatic OR gate [Fig. 2(b)] is composed of two microvalves connected in parallel. The pneumatic NAND gate shown in Fig. 2(c) is a universal logic gate (a gate from which any logical function may be built) that functions similarly to a NOT gate. For this logic gate, the output is false if both operand inputs are true, and the output is true in all other cases. Combinations of the AND, OR, and NOT gates are also capable of universal logic operations. For instance, the pneumatic XOR [Fig. 2(d)] is composed of a combination of NOT gates and OR gates. When only one of the operand inputs (A or B) is true, the Ctrl 1 input vacuum is transmitted to either X1e or X1f, resulting in a logic high output. When both operand inputs are true, the opening of valves X1a and X1d creates a direct connection between the Ctrl 1 input and two drilled holes to the atmosphere. In this case, neither X1e nor X1f is actuated, and no vacuum is transmitted to the output. The buffer amplifier circuit shown in Fig. 2(e) amplifies operand input vacuum signal and enables successful signal propagation in more complex pneumatic logic circuits. This pneumatic buffer circuit is based on the relation, $\text{NOT}(\text{NOT}(\text{A})) = \text{A}$. With both control inputs held at -87 kPa, application of a weaker vacuum to the operand input (A) opens valve b1. The opened connection to atmospheric pressure decreases the vacuum induced by the Ctrl 2 input, resulting in the closure of the valve b2. When valve b2 is closed, the full magnitude of the Ctrl 1 input is transmitted to the output.

As previously demonstrated [10], when the same vacuum magnitude (-87 kPa) is applied to the control and input channels of a single valve, the valve closes after the output channel has reached approximately 98% of the input and control vacuum. This feature was utilized for the development of bistable latching valve circuits. To characterize the pneumatic signal transduction through microvalves as a function of control channel pressure, individual valve input channels were supplied with a constant pressure of -87 kPa, whereas the pressure in the control channels was varied using a separate vacuum pump. The input channel vacuum (-87 kPa) applies a force to the membrane that resists the force applied by vacuum in the control channel. This results in an increased threshold for actuation and causes the valve to close prior to the transmission of the full input pressure to the output. Fig. 3(a) shows a linear increase in equilibrium output vacuum magnitude with increasing control vacuum magnitude, with the x-intercept representing the actuation threshold. Since the slope of this curve (1.5) is greater than 1, a linear network in which the output of valve n is the control input of valve $n+1$ will exhibit an exponential decrease in output vacuum magnitude with increasing n [Fig. 3(b)]. This imposes a practical limit on the integration of pneumatic logical structures that do not employ a signal amplification mechanism such as the buffer circuit described above. The elevation of actuation threshold induced by vacuum in the input channel was confirmed by measuring airflow through a single valve with -87 kPa applied to the input channel [Fig. 3(c)].

D. Binary Addition Circuits

Since binary addition is used in a wide range of computing operations including subtraction and multiplication, it plays an important role in the operations performed by the central processing unit of a modern computer [20]. In this paper, we demonstrate the feasibility of pneumatic binary addition circuits as a proof of principle for universal computing capabilities. Fig. 4 shows the logic diagram and truth table of a binary full adder. The operand inputs (A, B, and Carry In) are processed by a circuit of AND, OR, and XOR gates, resulting in two outputs—Sum and Carry Out. The truth table shows the expected logical outputs for all possible combinations of input

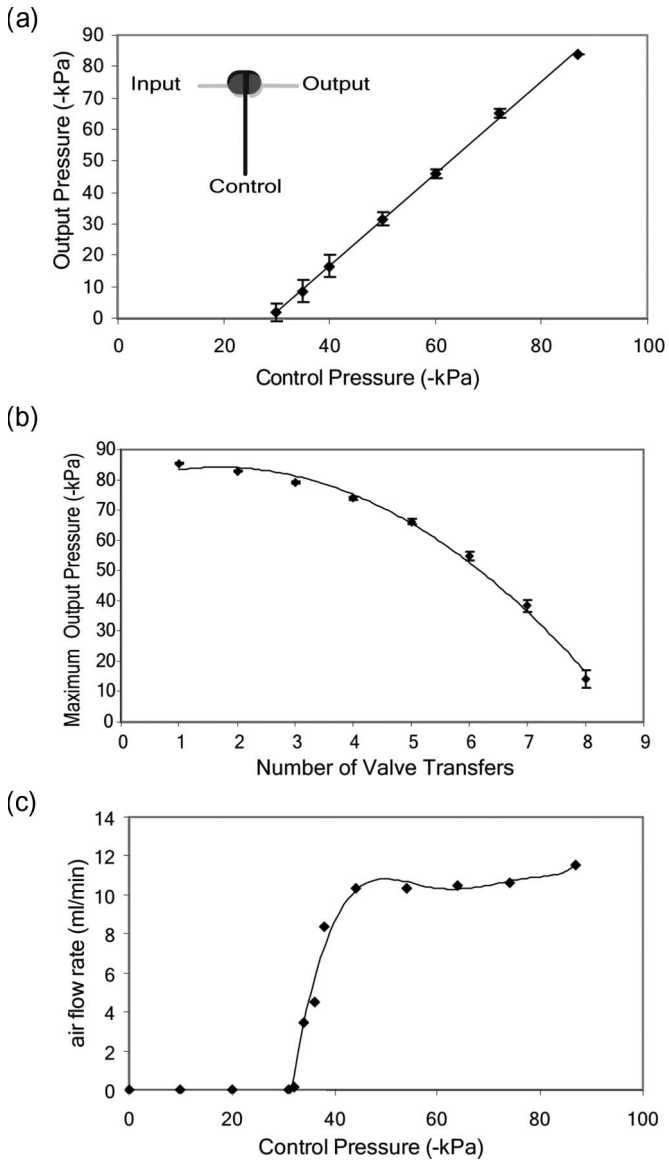
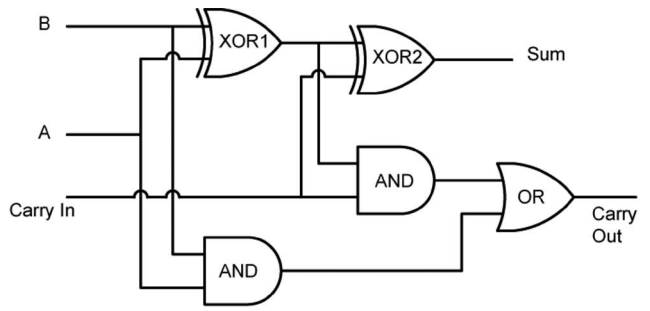


Fig. 3. (a) Impact of valve control pressure on output pressure for single valves held at constant −87 kPa input pressure. Output vacuum magnitude linearly decreases with decreasing control vacuum. In (b), a linear regression was used to illustrate signal loss in a nested valve array. Without amplification, signal strength exponentially decays as a vacuum is transferred between the output and control channels of a series of valves with fixed input channel pressures (−87 kPa). In (c), output airflow rates as a function of control input pressure show a steep transition at −32 kPa, the threshold for valve actuation with a fixed −87 kPa input pressure.

values. The pneumatic full adder (Fig. 5) is composed of two XOR gates and a hybrid OR gate in which two AND gates are aligned in parallel. Four gate control inputs (Ctrl X1, Ctrl X2, Ctrl X1X2, and Ctrl C) are required for the operation of this circuit. From the resting state in which each valve is closed, all of the operand and control gate inputs are simultaneously actuated with the exception of Ctrl X2 which is actuated after a 250-ms delay. This delay is necessary since the XOR2 gate processes the output of XOR1, which has a corresponding gate delay.

In a ripple-carry adder, multiple full adders are chained together with the Carry Out of one adder connected to the Carry In of the next most significant adder. Fig. 6 shows



A	B	Carry In	Sum	Carry Out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Fig. 4. Logic gate diagram and truth table for a full adder. A full adder processes a Carry In input along with two operand inputs (A and B) to generate a Sum and Carry Out.

the schematic layout of a pneumatic 4-bit ripple-carry adder. During carry propagation, the pneumatic Carry Out of an adder passes through a 2-mm diameter via hole in the PDMS membrane before actuating valves in an adjacent adder as the carry input. Each X1X2 control input is connected on-chip through a channel network that leads to a single drilled input hole. A similar bus input system was designed for the Ctrl C inputs, whereas the X1 and X2 control inputs were separately combined using off-chip tubing. Since each of the full adder control inputs is supplied with pneumatic signals in parallel through bus channels or off-chip tubing, only four off-chip controllers are required to actuate all of the control inputs of multibit adders. The output channels for sums and the final Carry Out convey pneumatic signals to a linear array of valves used as a readout of the computed sum. Half adders were incorporated into the circuits for addition of the least significant bits in the multibit adders.

In the 8-bit pneumatic ripple-carry adder (Fig. 7), a similar bus architecture is used to actuate the control inputs of the adders in parallel. The adders are radially arrayed with output channels for sums and the final carry extending to a linear array of readout valves in the center of the chip. A buffer amplifier circuit was added to the Carry Out of the fourth adder to amplify the signal and ensure successful carry propagation through any number of the adders.

III. Results

A. Basic Logic Gates

The propagation times and output magnitudes of each individual logic gate in Fig. 2 were characterized on a single fabricated device (supplemental materials). For each logic gate, operand and control inputs were simultaneously actuated. Each

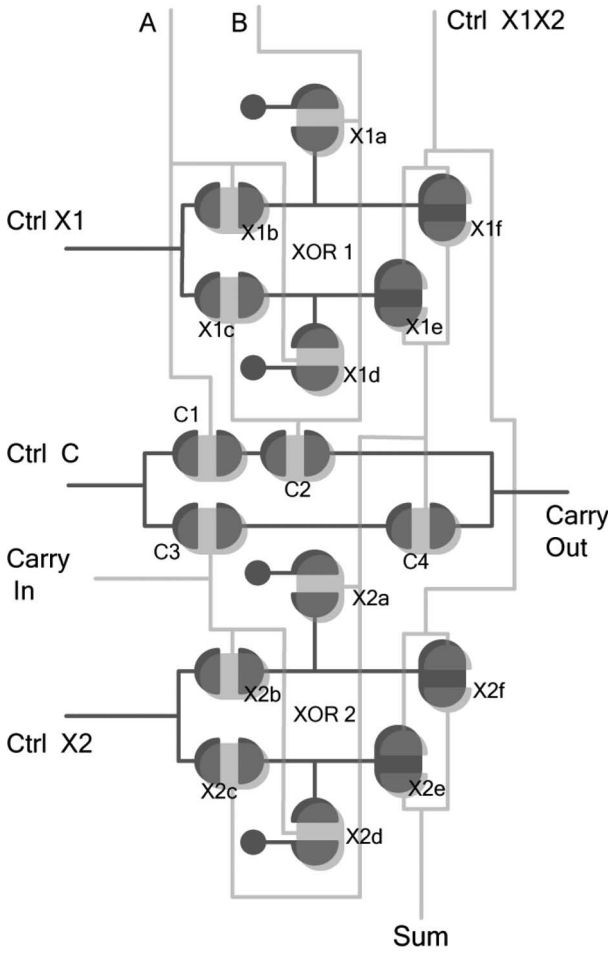


Fig. 5. Layout of a pneumatic full adder. Four control inputs (Ctrl X1, Ctrl X2, Ctrl X1X2, and Ctrl C) for constant vacuum are required for the operation of the circuit. The pneumatic full adder processes a Carry In input along with two operand inputs (A and B) to generate a Sum and Carry Out. Valves X1a–X1f and X2a–X2f form the XOR1 and XOR2 gates, respectively, that are shown in Fig. 4.

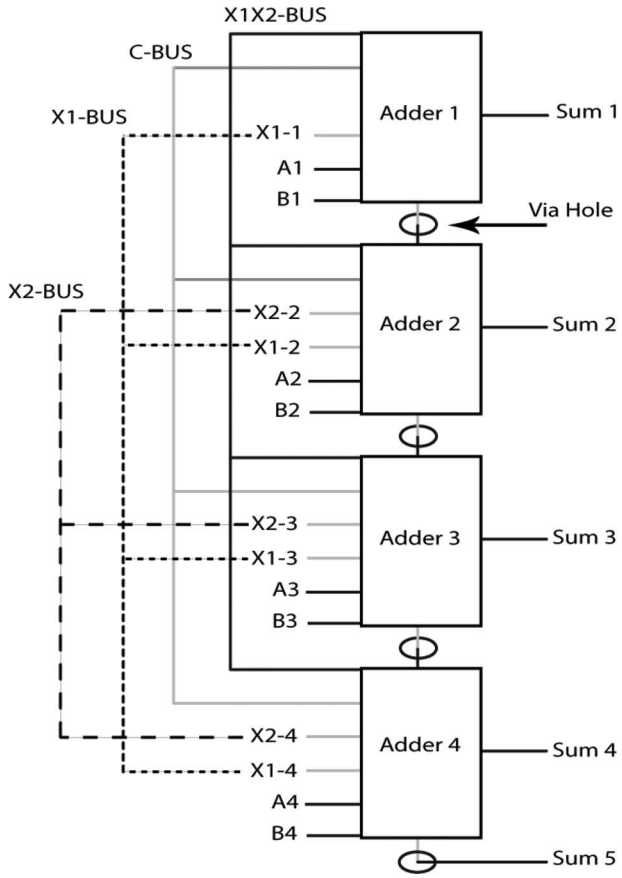


Fig. 6. Schematic layout of a pneumatic 4-bit ripple-carry adder. Black and gray solid lines represent channels on opposite sides of the PDMS membrane, whereas dashed lines represent off-chip tubing connections. Carry propagation occurs in the direction from Adder 1 to Adder 4, passing through via holes in the PDMS membrane.

logic gate generated output vacuum magnitudes that fall into the correct ranges for logic high or logic low, as defined above. The lowest magnitude for a logic high output was observed for the XOR gate (−63 kPa) since it is composed of the most complex network of valves. Latching of the output vacuum occurs in the XOR gate if all of the inputs are simultaneously turned off. This latched volume would be eventually restored to atmospheric pressure due to the gas permeability of the PDMS membrane; however, the process can be expedited by actuating the operand inputs while the control inputs are closed. Dynamic response times were defined as the interval between the actuation of off-chip solenoid valves and the opening of an output microvalve due to a logic high output. Response times were determined using CCD camera videography. The longest response time (250 ms) was observed for the XOR gate. Since these response times include a delay due to the evacuation of tubing between the solenoid valves and the chip inputs, optimization of vacuum pump speed and the dimensions of off-chip tubing may significantly improve the speed of logical operations.

Pressure transfer characteristics evaluated for the pneumatic inverter indicate sharp threshold transitions between high and low output for a wide range of gate control input pressures (supplemental materials). Actuation of the inverter microvalve opens a low resistance path between the output and a drilled hole to atmosphere, resulting in a highly effective reduction of output vacuum magnitude to subthreshold levels.

TABLE I
TRUTH TABLE FOR PNEUMATIC FULL ADDER IN KILOPASCALS

A	B	Carry In	Sum	Carry Out
6	6	6	0	0
-87	6	6	-46	0
6	-87	6	-48	0
-87	-87	6	0	-65
6	6	-87	-64	0
-87	6	-87	0	-55
6	-87	-87	0	-54
-87	-87	-87	-65	-65

B. Pneumatic Full Adder

Table I shows the output vacuum and pressure magnitudes of the pneumatic full adder for all possible combinations of inputs. As an example, the Carry Out is true when both XOR (A, B) and the Carry In are true. In these cases, the output of XOR1 is transferred to the control input of valve C4 (Fig. 5). The input

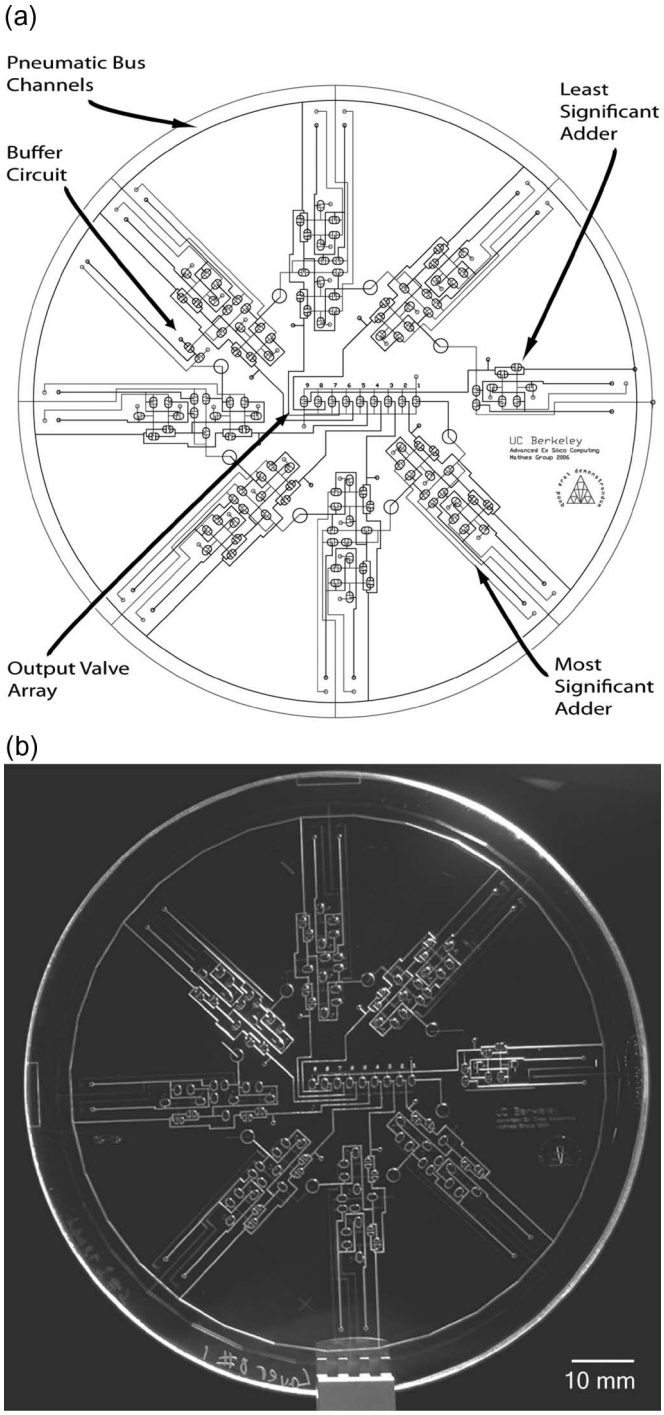


Fig. 7. (a) Layout and (b) photograph of the 8-bit pneumatic ripple-carry adder. Circular channels along the perimeter are bus channels that supply pneumatic signals to each Ctrl C and Ctrl X1X2 gate input. The adders are radially arrayed with the least significant adder on the far right and carry propagation occurring in the counterclockwise direction. The Sum output of each adder and the final Carry Out actuate the output display valves in a linear array. A buffer circuit was added to amplify the pneumatic Carry Out signal of the fourth adder.

of this valve is supplied with approximately −87 kPa signal via the Ctrl C gate input channel. Based on the −64 kPa logic high output of an individual XOR gate, and using the equation for the linear regression in Fig. 3(a), a Carry Out vacuum of −54 kPa is predicted. This precisely agrees with the experimentally determined values from the pneumatic full adder. The

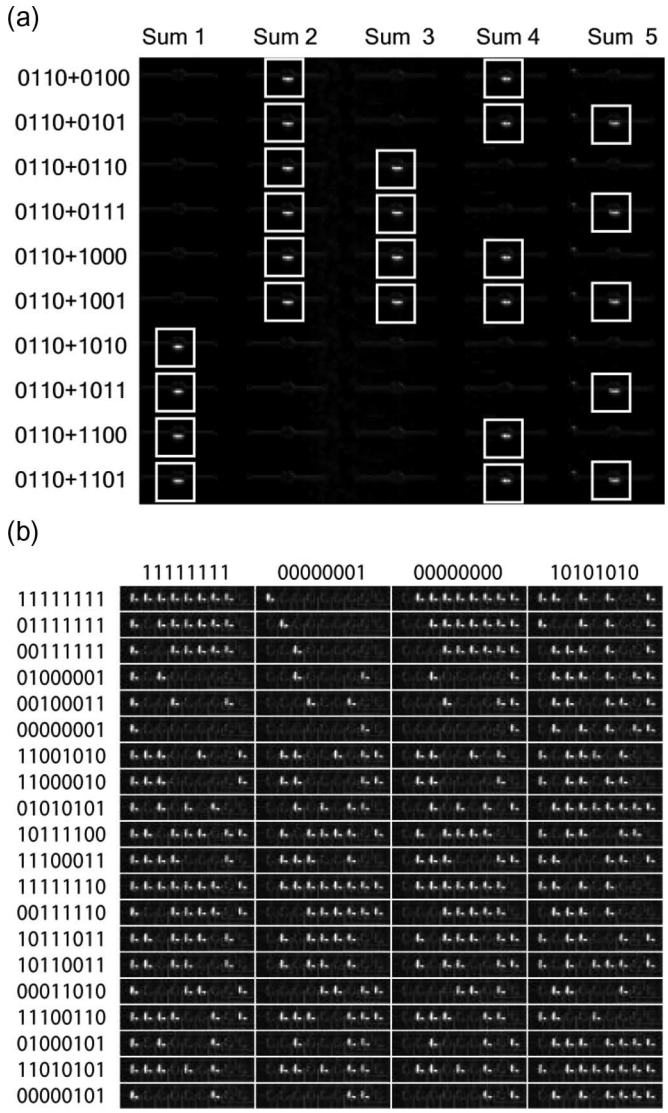


Fig. 8. Video frames showing the linear output valve array (a) of the 4-bit pneumatic ripple-carry adder and (b) of the 8-bit pneumatic ripple-carry adder after computing the sums of the indicated inputs. Open valves reflect more light and appear brighter than closed valves.

operation of the full adder required a 250-ms delay for the actuation of the X2 control input. Delays less than 250 ms were insufficient for the transfer of output from XOR1 to the input of XOR2 and, therefore, resulted in incorrect output sums. To avoid latching of gates within the adder, an eight-step 2-s closing procedure is used to expedite a return to the resting state (see supplemental materials). More complex closing procedures are not required for multibit adders since the closing program can be applied to each adder in parallel. No vacuum is transmitted to the Carry Out or Sum outputs during these closing procedures.

C. Multibit Adders

Fig. 8(a) shows selected outputs of the pneumatic 4-bit binary adder. Each row is a digital image of the output valve array taken after actuation with the indicated pattern of inputs. Open valves reflect more light and appear brighter than closed valves. Simultaneous actuation of all inputs except the X2

bus results in the automatic propagation of carry information throughout the system. The addition of 1111 and 0001 generates a carry in the least significant bit that is propagated through all of the other adders and results in the output sum of 10 000. This represents a worst case scenario for the time required to compute a sum and was used to determine a reliable actuation delay for the XOR2 bus. Correct outputs were reliably obtained for each of the 256 possible pneumatic input configurations using a 500-ms XOR2 actuation delay.

Fig. 8(b) shows the output of several random inputs and worst case scenarios of carry propagation for the pneumatic 8-bit adder. The control inputs of the buffer circuit were powered by constant vacuum during the operation of the device, and a 1.1-s delay was used for the actuation of the X2 bus input. Previous designs that did not include the amplifier structure failed due to loss of signal during carry propagation. The need for signal amplification is due to the large number of serial valve transfers that occur during carry propagation and can be predicted based on the signal transduction data presented in Fig. 3. Particularly challenging cases arise when a weak carry signal must open a valve closed with a vacuum applied to its input channel. This is the case during the computation of 01111111 + 00000001 in which valve X2f is opened in the most significant adder by a propagated carry signal. Digital videos of the carry propagation through the 4- and 8-bit adders can be found in the online supplemental materials.

IV. Discussion and Conclusion

We have developed a technology for the design, fabrication, and testing of complex integrated digital logic structures using networks of normally closed pneumatically actuated microvalves. These microvalves were shown to function like the transistors in conventional transistor–transistor logic circuits. Here, we have demonstrated that these pneumatic "transistors" can be assembled into a variety of basic gate structures (AND, OR, NOT, NAND, and XOR) and shown that they can be combined using standard design principles to form computational circuits for binary addition. The development of an amplifying buffer circuit has allowed the extension of the technology to 8-bit binary adder circuits in which pneumatic signals must propagate through numerous gates. This result suggests that more complex logical circuits such as the significantly faster carry-lookahead adder [21] could be developed using the design principles demonstrated here.

Future modeling of the mechanics of individual microvalves and further characterization of airflow through microvalve networks will allow precise optimization for improved response times. It has been noted that pneumatic logical devices are limited by the speed of sound in air [11]. Although this limitation has prevented any serious competition with digital electronics for computing speed, actuation frequencies in the millisecond scale are commonly used in lab-on-a-chip devices and should be attainable using micropneumatic logic. Furthermore, the miniaturization and integration of control systems may be particularly useful for the development of portable microelectromechanical system devices for pathogen detection [22], [23] or extraterrestrial biomarker analysis [24].

The timing of valve actuation can be integrated using micropneumatic logical structures. As the carry propagates through a multibit micropneumatic adder, an automatic series of valve actuations occur in a precise time sequence. Similarly, in digital electronics, delay circuits are often used to synchronize operational sequences in signal processing units [25]. As previously noted, the latching behavior of microvalve networks developed by our group resembles the function of simple memory circuits such as flip-flops [10]. These features could be exploited in future integrated systems that implement dynamic logical control. For situations in which latching behavior is disadvantageous, channels joining microvalves in a network can be modeled as an *RC* circuit with a capacitance and resistance to the ground (atmospheric pressure). Smaller microvalves and channels would decrease the network capacitance, and nanoscale leak channels or membranes with altered gas permeability may increase airflow to the latched volumes from the atmosphere without significantly decreasing output signals during a logical operation. Such a system for reducing the latching characteristics of microvalve networks will result in improved performance and obviate the closing procedures required here.

Integrated pneumatic logic structures have already proven useful for the development of latching structures and multiplexed control of valve arrays in complex lab-on-a-chip applications [10]. Further development in this area will catalyze progress toward the creation of multipurpose programmable microfluidic devices that can be utilized for diverse analyses. Miniaturized pneumatic logic structures may also allow integrated control in microassembly and microrobotic systems which often employ pneumatic actuation mechanisms [26], [27]. Furthermore, this technology could be utilized to develop simple computing systems that are immune to radio frequency or pulsed electromagnetic interference [28]. Such computing devices may also be useful in extreme environments such as those of space missions with controlled pressure environments, where cosmic rays result in the malfunction or failure of electronic components [29].

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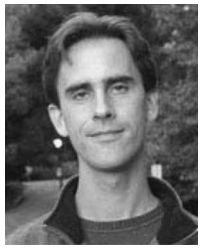

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